Digital, Analog and RF Design Opportunities of Three-Independent-Gate Transistors

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Abstract— Field-Effect Transistors (FETs) with Three Independent Gates (TIG) can achieve different modes of operation according to the bias of the gate terminals. In particular, TIG FETs were recently shown capable of (i) device-level polarity control, (ii) dynamic threshold modulation and (iii) subthreshold slope tuning down to ultra-steep-slope operation. Experimentally demonstrated using both contemporary FinFETs and emerging silicon nanowires channel technologies, TIGFETs unlock several design opportunities. In this paper, we comment on the digital, analog and RF design capabilities offered by this new class of transistors.

I. INTRODUCTION

In order to sustain the ever-increasing need for computing performance, the semiconductor industry introduced many device-level innovations during the last decade. On the one hand, novel device geometries, such as the Intel’s tri-gate transistor, a.k.a. FinFETs [1], or the Fully-Depleted Silicon-on-Insulator (FDSOI) transistor [2] technologies, have been successfully employed to improve the current density, reduce the leakage floor and reduce the short-channel effects at advanced technology nodes. On the other hand, complex materials, such as high-κ gate stacks, silicon-germanium channels or copper-based interconnects were additionally leveraged to allow the device scalability down to the contemporary 14 nm technology node [1]. Even though the transistor structure has seen a strong evolution, the basic operation principle, i.e., thermionic emission, remains unchanged since the introduction of Complementary Metal-Oxide-Semiconductor (CMOS) logic.

In parallel to the focus on scaling, an interesting approach consists in increasing the functionalities of the basic transistors by means of additional gate [3]–[7]. In particular, a device exploiting silicided contacts and additional gate terminals to bias the Schottky barriers at source and drain has been recently shown capable of achieving different modes of operation including: (i) The dynamic reconfiguration of the device polarity (n- or p-type) [4]; (ii) The dynamic control of the threshold voltage (V_T) that does not lead to any detriment of the on-state current [5]; And (iii) the dynamic control of the Subthreshold Slope (SS) allowing to trigger weak impact ionization and record an average SS of 6 mV/dec over 5 decades of current swings [6].

In this paper, we make the link between the capabilities of Three-Independent-Gate (TIG) FET devices and their potential for digital, analog and RF design. The remainder of this paper is organized as follow. Section II introduces the main results regarding TIGFET device fabrication. Section III reviews the main opportunities of this technology in terms of digital arithmetic design, while Section IV and Section V discuss the possible research avenues offered by this novel technology in the field of high-performance analog and RF design. Section VI concludes the paper.

II. THREE-INDEPENDENT-GATE FIELD EFFECT TRANSISTORS

TIGFETs have been implemented and characterized using either conventional FinFET-like structures or more advanced vertically-stacked NanoWire (NW) FET [4]–[6]. Without loss of generality, we first report the main fabrication process steps employed to realize TIG NWFETs. Then, we comment on the operation of the device.

A. Device Fabrication

Fig. 1-a shows the conceptual structure of a TIGFET. The device exploits vertically-stacked nanowires as channel and metallic source and drain contacts. The channel electrostatics is controlled by three electrodes: The Polarity Gate at Source (PG_S) and the Polarity Gate at Drain (PG_D) modulate the Schottky barriers at source and drain; The Control Gate (CG) controls the potential barrier in the channel and turns the device on or off.

The TIGFET is fabricated with a dopant-free process on an SOI wafer [4]–[6]. The vertically-stacked nanowires are realized using a single deep reactive ion etching step [4] that results in a stack of 4 nanowires with length and diameter of 350 nm and 50 nm, respectively. After a 15 nm SiO₂ gate dielectric formation, two Gate-All-Around (GAA) 120 nm polysilicon structures are deposited to form PG_S and PG_D. CG is subsequently self-aligned to them. Finally, NiSi silicide is formed on the source and drain pillars to create mid-gap
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in Fig. 2-c and Fig. 2-d for both a) and high-V made for behave as a high-V band bending at the Schottky contacts prevents both electron obtain a lower leakage floor than in Fig. 2-a, as the opposite terminals and leads to ultra-low-leakage states [5]. Fig. 2-b simultaneously cut off the carrier injections at both source and drain independent Schottky biasing gives the possibility to simultaneous operation leads to an individual control of the device polarity. CG traditionally controls the device bias leads to hole conduction and results in electron conduction at the source and drain Schottky barriers, barriers by the PG

B. Polarity and Threshold Control

In a TIGFET, the control of carrier injection at the Schottky barriers by the PGs and PGD gate terminals offers the capability to determine the operation modes of the device. Fig. 2-a presents a conceptual band diagram, when PGs and PGD are controlled by the same potential. A positive PGs/D bias enables electron conduction at the source and drain Schottky barriers, setting the device polarity to n-type, while a low PGs/PGD bias leads to hole conduction and results in p-type behavior. CG traditionally controls the device on and off. The mode of operation leads to an individual control of the device polarity. When the two PG terminals are biased separately, the independent Schottky biasing gives the possibility to simultaneously cut off the carrier injections at both source and drain terminals and leads to ultra-low-leakage states [5]. Fig. 2-b presents the associated band diagrams for an n-type conduction where PGs controls the device on and off. In this case, we obtain a lower leakage floor than in Fig. 2-a, as the opposite band bending at the Schottky contacts prevents both electron and hole injection into the channel. As a result, the device will behave as a high-V_T transistor. Similar considerations can be made for p-type conduction. Note that the low-V_T (Fig. 2-a) and high-V_T (Fig. 2-b) configurations share the same on state, reducing performance degradation. This property is not achievable in conventional multi-V_T techniques.

The performances obtained on a fabricated device are shown in Fig. 2-c and Fig. 2-d for both n- and p-type conduction respectively. A threshold difference of 0.86 V is observed. The high-V_T off-state current reaches 1 pA compared to 4.6 pA in low-V_T. Full characterization of n- and p-branches can be found in [5].

C. Steep Slope Control

In addition to the previous properties, this device can also be operated as a Super-Steep-Subthreshold-Slope FET (S^4-FET). The operation of the S^4-FET mode is illustrated in Fig. 3-a. The application of a positive bias potential VPGD creates a potential well under the gate and is key to obtain a steep-slope behavior as shown in [6]. When electrons acquire enough energy, weak impact ionization is triggered and electron/hole pairs are generated (step 1). The generated holes accumulate in the potential well under the gate (step 2). This lowers the barrier and provides more electrons for impact ionization, thus establishing a positive feedback. During the transition, the energy band in the PG regions is lowered (step 3), maintaining the potential well for the accumulation and improving the average SS over the subthreshold region. While Fig. 3-a only represents an n-type configuration, p-type configuration can be achieved by applying a negative VPGD potential [6].

Fig. 3-b reports the characteristics of a TIG FET operated in S^4-FET mode, carried out at room temperature [6]. Note that a fin-based channel geometry is used in the measured device. Minimum SS of 3.4 mV/dec is achieved. An average SS of 6.0 mV/dec is observed for 5 decades of current. Complete n-type and p-type characteristics at both room and low temperatures are available in [6], [8].

The different modes of operation available in TIGFET lead to many circuit design opportunities as illustrated in the next sections.

III. DIGITAL DESIGN OPPORTUNITIES

The performance of arithmetic logic is critical to contemporary circuit design. Exclusive-OR (XOR) and MAJority (MAJ) logic functions are extensively used in arithmetic circuits. Consequently, their physical realization is of paramount importance. In this context, TIGFETs open up new implementation opportunities with a small number of resources unachievable with conventional CMOS technologies [9], [10]. Based on transmission-gates, the implementation of 3-input XOR and 3-input MAJ gates, depicted in Fig. 4, enables a full-adder realization with only 8 devices (input inverters apart) and only
one transistor per stack. The full-adder forms a fundamental building block for many arithmetic circuits.

In addition to providing larger capabilities for arithmetic operators, TIGFETs lead to simpler multi-\(V_T\) circuit design. While traditional multi-\(V_T\) circuits require extra technological steps to co-integrate devices with different threshold voltages [11], the TIGFET technology supports the two \(V_T\) configurations in a unique device, enabling to a drastic fabrication cost reduction. Fig. 5 illustrates two different NAND gate realizations for HP and LL applications, implemented with only 3 transistors. In Fig. 5-a, a High-Performance (HP) gate is obtained by connecting inputs to the CGs of \(p\)-FETs. Thus, the performance for pulling the logic gate up is improved by applying the low-\(V_T\) configuration of the devices (solid line in Fig. 2-d). In contrast, the Low-Leakage (LL) gate (Fig. 5-b) is obtained by controlling the \(p\)-FETs from the PGD. Leakage power is thereby reduced by forcing the devices into HV\(_T\) operation (dash line in Fig. 2-b). In both HP and LL gates, PG\(_S\) and CG of the \(n\)-type TIGFETs are connected to input signals, combining 2 regular CMOS transistors in only one TIGFET [11].

We refer the interested reader to [12] for more TIGFETs opportunities in digital design, such as embedded power gating or compact flip-flop.

**IV. ANALOG DESIGN OPPORTUNITIES**

Analog circuit performance is fundamentally linked to transistor figures of merit including transconductance efficiency (\(g_m/I_D\)), transit frequency (\(g_m/C_{gs}\)), and intrinsic gain (\(g_m/g_{ds}\)) [13]–[15]. These metrics dictate constraints in the power consumption, speed, and gain of analog circuits. Power efficiency, for instance, involves a tradeoff between the bias current required to achieve a certain transconductance (\(g_m/I_D\)), and the resulting device capacitance that contributes to circuit loading (\(g_m/C_{gs}\)). For CMOS transistors operating in weak inversion, \(g_m/I_D\) is directly coupled to Subthreshold Slope (SS) by:

\[
\frac{g_m}{I_D} = \frac{1}{I_D} \cdot \frac{\partial I_D}{\partial V_g} = \frac{\partial (\ln I_D)}{\partial V_g} = \frac{\ln(10)}{SS} \tag{1}
\]

This limit results from the physics of thermionic emission and gate control of surface potential. With perfect surface potential control, a MOSFET could achieve \(g_m/I_D \leq 40\) S/A (SS \(\geq 60\) mV/decade), but this is not practical due to finite depletion capacitance. Transistor scaling has led us to very fast transistors (high \(g_m/C_{gs}\)), resulting in more and more analog designs being pushed toward subthreshold operation in order to leverage the enhanced power efficiency (high \(g_m/I_D\)).

Measurements of Fig. 3-b show SS as steep as 3.4 mV/dec, giving the potential for \(g_m/I_D = 677\) S/A, which could result in a 25 x power efficiency improvement for a wide range of analog circuits. A compelling, ubiquitous application is to replace the input pair of a CMOS differential amplifier with steep-slope TIGFETs. However, several challenges still have to be overcome before reaching such a level of performance. Indeed, a circuit challenge is to reliably bias the TIGFETs in the steep slope region, which can be achieved through replica biasing techniques and tight control of \(V_{DS}\) through active cascode structures. Other challenges to be addressed through a combination of device and circuit engineering include noise, capacitance, finite \(g_{ds}\), and reducing the required \(V_{DS}\) required to achieve steep SS.

**V. RF DESIGN OPPORTUNITIES**

Many THz detection approaches have been developed to-date [17]. However, a miniaturized room-temperature detector technology, exhibiting a very sensitive THz response, is still largely missing.

Conventional MOSFETs can operate as efficient THz detectors far beyond their fundamental cut-off frequency [16]. Indeed, FETs can operate as non-resonant broadband THz detectors with high responsivity, as described by the Dyakonov-Shur theory. When a THz field is applied between the gate and the source terminal of the transistor, the THz electric field is rectified, like in square-law detectors, and a DC source-to-drain photo-voltage is induced. This voltage difference \(\Delta U\), called the detector photoresponse, can be expressed as a function of \(V_{GS}\) for a fixed drain bias by [18]:

\[
\Delta U = \frac{1}{4} \cdot \frac{1}{\sigma} \cdot \frac{d\sigma}{d\theta} \Big|_{U=V_{GS}} = \frac{1}{4} \cdot \frac{1}{dV_{GS}} \ln (I_{DS}(V_{GS})) \tag{2}
\]

Eq. (2) assumes conjugate matching of an antenna coupling the incoming THz radiation into the device and an infinite load impedance (from drain to source), i.e., \(Z_L = +\infty\). Therefore, it provides an upper bound for the detector photoresponse. Thanks to this simple physical model, we can evaluate the potential of the TIGFETs for THz detection applications.

We estimate the maximum attainable current responsivity \(R_i\) (\(R_i = \Delta U G_{DS}/P_n\)) where \(G_{DS}\) represents the drain-to-source conductance) from the measured device characteristics.
TIGFETs have demonstrated a large versatility of operations in the domain of digital, analog and RF design. At room temperature (Fig. 3-b), the results of our calculations are depicted in Fig. 6. For the purpose of estimating the current-responsivity, the device $I - V_{GS}$ characteristics were fitted to a model of the form [19]. It is observed that TIGFETs can achieve a much larger responsivity compared to a regular FET. While the maximum current-responsivity of regular thermally-limited FET detectors is in the order of $R_I \approx 10 \text{A/W}$, TIGFETs can enable room-temperature current-responsivities up to 2 orders of magnitude larger, promising THz detectors with performances unachievable with regular FET (and also Schottky diode) technologies.

In order to estimate the Noise Equivalent Power (NEP) in TIGFET detectors, it is important to analyze the different sources of noise in such devices. Overall, the electrical noise can be divided into a thermal contribution and an excess part: $S_V = S_{V,T} + S_{V,ex}$, where the excess part consists of: (a) $1/f^\alpha$-type flicker noise ($\alpha = 1$), and (b) generation-recombination-type noise, which varies as $1/f^2$. There are essentially two physical mechanisms behind any fluctuations in electrical current: (1) fluctuations in the mobility, and (2) fluctuations in the number of carriers. In general, the excess noise can be attributed to carrier number fluctuations stemming from charge carrier capture, release and recombination events. In FinFETs as well as TIGFETs, the charge fluctuation in the gate dielectric could also induce fluctuations of the carrier mobility, giving rise to so-called Correlated Mobility Fluctuations (CMF). When analyzing all noise contributions, it is found that $1/f$ noise mostly originates from the CMF due to trapping/de-trapping of channel carriers into slow gate dielectric traps [20], [21]. Our estimates for all the noise contributions in the TIGFET, under the bias conditions at which maximum responsivity is attained, show that generation-recombination and flicker noises dominate over thermal noise, as also observed by other authors [22], [23]. The total (current) noise spectral density is estimated to be on the order of $10^{-22} \text{A}^2/\text{Hz}$, which leads to projected NEP levels on the order of $10^{-14} \text{W}/\text{Hz}^{0.5}$, thus 2 orders of magnitude better performance than current room temperature THz detectors.

VI. CONCLUSION
In this paper, we evaluated the opportunities given by TIGFETs in the domain of digital, analog and RF design. TIGFETs have demonstrated a large versatility of operations with the possibility to implement, in addition to a regular MOS transistor behavior, the following functionalities: (i) a device-level polarity control, (ii) a multi-$V_T$ control scheme and (iii) ultra-steep-slope mode. While the first 2 modes of operations have largely been investigated in literature for digital design, we further looked into the possible benefits of TIGFETs in analog and RF design and identified that they could result in a $25 \times$ power efficiency improvement for analog circuits and in 2 orders of magnitude more sensitive THz detectors.

REFERENCES